IN THE CLAIMS:

Please amend claims 1, 10, 16, and 22 as shown in the complete list of claims that is presented below.

1. (currently amended) A semiconductor package ~~which has~~ for a semiconductor chip, said semiconductor package having a surface with ~~a plurality of connection terminals to be connected to wiring on a board and~~ a plurality of test terminals ~~that are~~ for use during testing of said semiconductor chip and with a plurality of connection terminals for connection to wiring on a board after testing, said test terminals being electrically isolated from ~~he~~ said wiring on said board,

wherein said connection terminals are arranged in a first area at predetermined pitches in a lattice and said test terminals are arranged in a second area at pitches narrower than said predetermined pitches in a lattice.

2. (original) The semiconductor package according to claim 1, wherein said connection terminals and said test terminals are formed by solder balls.

3. (original) The semiconductor package according to claim 1, wherein said connection terminals and said test terminals are formed by lands.

4. (previously presented) The semiconductor package according to claim 1, wherein said second area is placed in the center of said surface, and said first area is placed in the periphery of said surface so as to surround said second area.

5. (original) The semiconductor package according to claim 4, wherein said connection terminals and said test terminals are formed by solder balls.

6. (original) The semiconductor package according to claim 4, wherein said connection terminals and said test terminals are formed by lands.

7. (previously presented) The semiconductor package according to claim 1, wherein said second area is placed in the periphery of said surface, and said first area is placed so as to surround said second area.

8. (original) The semiconductor package according to claim 7, wherein said connection terminals and said test terminals are formed by solder balls.

9. (original) The semiconductor package according to claim 7, wherein said connection terminals and said test terminals are formed by lands.

10. (currently amended) The semiconductor package according to claim 7, wherein said second area is placed where a high-heat-buildup circuit is disposed.

11. (original) The semiconductor package according to claim 10, wherein said connection terminals and said test terminals are formed by solder balls.

12. (original) The semiconductor package according to claim 10, wherein said connection terminals and said test terminals are formed by lands.

13. (original) The semiconductor package according to claim 1, wherein said first area is formed in a plurality of places, and said second area is placed so as to isolate said first areas respectively formed in said plurality of places from each other.

14. (original) The semiconductor package according to claim 13, wherein said connection terminals and said test terminals are formed by solder balls.

15. (original) he semiconductor package according to claim 13, wherein said connection terminals and said test terminals are formed by lands.

16. (currently amended) A semiconductor package ~~which has~~ for a semiconductor chip, said semiconductor package having a surface with a plurality of connection terminals to be connected to wiring on a board and with a plurality of test terminals for testing ~~circuitry within the package~~ the semiconductor chip before the connection terminals are connected to the wiring on the board and ~~to be connected~~ for connection to a ground on the board when the connection terminals are connected to the wiring on the board,

wherein said connection terminals are arranged in a first area at predetermined pitches in a lattice and said test terminals are arranged in a second area at pitches narrower than said predetermined pitches in a lattice.

17. (original) The semiconductor package according to claim 16, wherein said connection terminals and said test terminals are formed by solder balls.

18. (original) The semiconductor package according to claim 16, wherein said connection terminals and said test terminals are formed by lands.

19. (previously presented) The semiconductor package according to claim 1, wherein said surface is rectangular and said second area is placed in the four corners of said rectangular surface, and said first area is placed in an area except for said four corners.

20. (original) The semiconductor package according to claim 19, wherein said connection terminals and said test terminals are formed by solder balls.

21. (original) The semiconductor package according to claim 19, wherein said connection terminals and said test terminals are formed by lands.

22. (currently amended) A lead-type semiconductor package ~~which has~~ for a semiconductor chip, said semiconductor package having a plurality of ~~connection leads to be connected to wiring on a board and a plurality of~~ test leads ~~that are~~ for use during testing of said semiconductor chip and having a plurality of connection terminals for connection to a wiring board after testing, said test terminals being electrically isolated from the wiring on said board,

wherein said connection leads are arranged at predetermined pitches, and said test leads are arranged at pitches narrower than said predetermined pitches.

23. (previously presented) A semiconductor device having the semiconductor package of claim 1, in combination with the board and mounted on the board.

24. (previously presented) A semiconductor device having the semiconductor package of claim 16, in combination with the board and mounted on the board.

25. (previously presented) A semiconductor device having the semiconductor package of claim 22, in combination with the board and mounted on the board.